PMX-P and PME-P

User's Manual

XMC or PCIe to PCI/PCI-X Adapters

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Release 2.1
April 29, 2014

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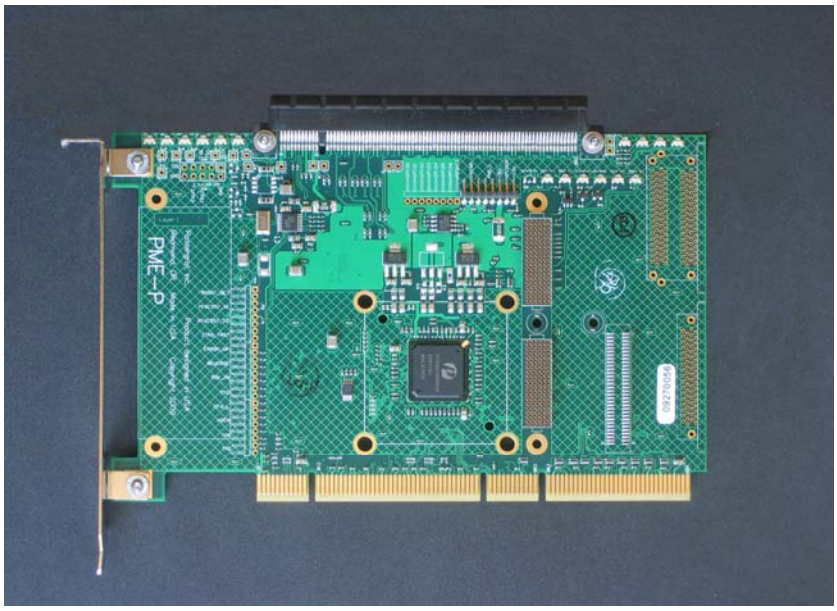

PME-P

Introduction

This manual provides information about how to configure, install, and program the Rastergraf PMX-P and PME-P PCI Express to PCI/PCI-X Adapters for 32-bit and 64-bit computers with PCI or PCI-X slots. For the sake of brevity, the term PMX/PME will be used when referring to the two boards collectively. PCI-X is a plug-compatible high performance superset of PCI and allows the bus speed to operate at up to 133 MHz.

This manual is broken down into five chapters:

Chapter 1: General Information
Chapter 2: Specifications
Chapter 3: Connector Pinouts and Cable Information
Chapter 4: Installing Your PMX-P or PME-P Adapter Board
Chapter 5: Troubleshooting

Chapter 1 provides background material about the PMX/PME boards, and it is not essential for the hardware or software installation. If you want to perform the installation as quickly as possible, start with Chapter 4. If you have problems installing the hardware, refer to Chapter 5 for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf board. There may well be variables specific to your computer configuration that this manual does address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 6, “Troubleshooting”. If this information does not enable you to solve your problems, do one of the following:

1) call Rastergraf technical support at (541) 923-5530

2) send E-mail to support@rastergraf.com .

Board Revisions

This manual applies to the following board revision levels:

PME-P/PMX-P Fab Rev 0

Manual Revisions

Revision 1.0	November 10, 2009	First released version
Revision 2.0	September 7, 2010	Some revisions
Revision 2.1	April 29, 2014	Minor corrections

Notices

Information contained in this manual is disclosed in confidence and may not be duplicated in full or in part by any person without prior approval of Rastergraf. Its sole purpose is to provide the user with adequately detailed documentation to effectively install and operate the equipment supplied. The use of this document for any other purpose is specifically prohibited.

The information in this document is subject to change without notice. The specifications of the PMX-P and PME-P Adapter boards and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf assumes no responsibility for any errors or omissions that may occur in this manual. Customers are advised to verify all information contained in this document.

The electronic equipment described herein generates, uses, and may radiate radio frequency energy, which can cause radio interference. Rastergraf assumes no liability for any damages caused by such interference.

Rastergraf products are **not** authorized for ***any*** use as critical components in flight safety or life support equipment without the written consent of the president of Rastergraf, Inc.

These products have been designed to operate in user-provided PCI-compatible computers. Connection of incompatible hardware is likely to cause serious damage. Rastergraf assumes no liability for any damages caused by such incompatibility.

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Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

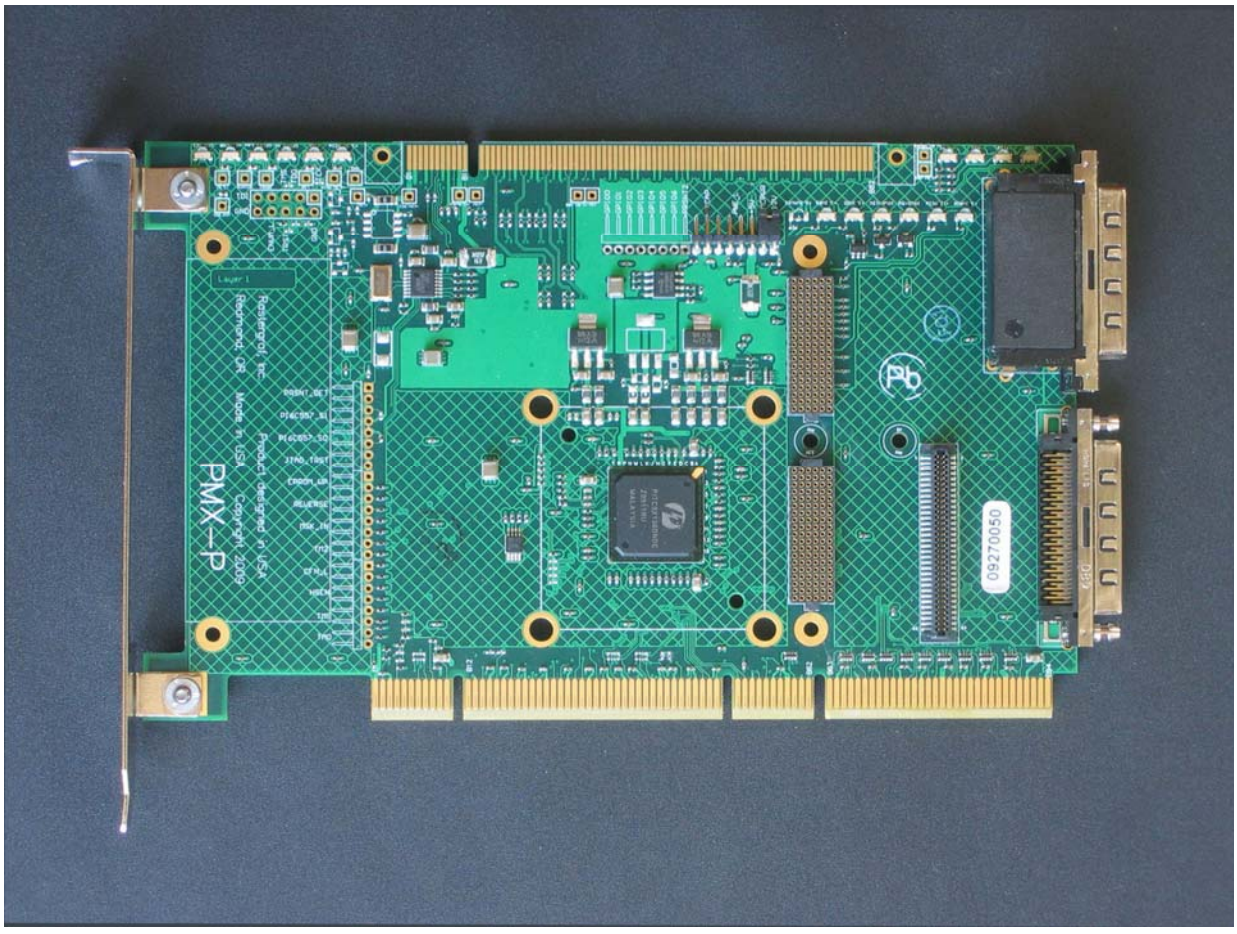
`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, or the hash-mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

Chapter 1
General Information



PMX-P

1.1 Introduction

The Rastergraf PMX-P and PME-P are part of Rastergraf's line of active and passive interface adapters and carriers for PCI and CompactPCI computers

The PMX-P carrier board enables an XMC module to be used in a PCI or PCI-X slot. Its design enables the PMX-P with XMC card installed to fit in one standard 32-bit or 64-bit PCI or PCI-X slot and allows adjacent slots in the computer to be occupied and for the computer to be completely closed up. Optional breakout connectors provide access to the Pn4 (PMC) and Pn6 (XMC) I/O connectors.

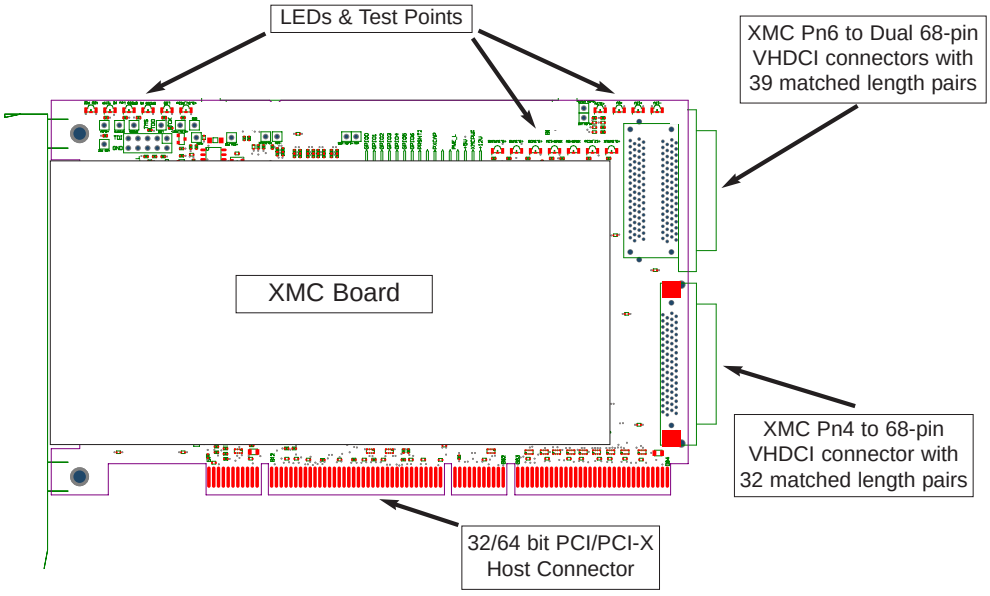
The PME-P carrier board enables a standard PCI Express (PCIe) board to be used in a PCI or PCI-X slot. Because the PCIe board plugs into a socket at the top edge of the PME-P, the height of the combination of the two boards stands at about twice the standard height of a PCI card. By necessity, therefore, the PME-P is most practically used in a lab environment, for testing, or other non-production applications.

Rastergraf produces several other PMC carriers for PCI or CompactPCI computers. For more information about them and the rest of Rastergraf's products, please contact Rastergraf Worldwide Sales at (541) 923-5530 or consult Rastergraf's web page at http://www.rastergraf.com.

1.2 PMX-P Feature Summary

- Short PCI form factor board holds one VITA 42.3 XMC card
- PMX-P/P46 version provides optional breakout connectors with matched-length pairs for PMC Pn4 and XMC Pn6
- 32/64-bit, 33/66/100/133 MHz PCI/PCI-X operation
- PCI 2.3 and PCI-X 1.0 compliant with Universal PCI signaling
- VITA 42.3 compliant supports PCIe x1, x2, or x4 on the XMC
- Uses Pericom PI7C9X130 PCI Express to PCI/PCI-X Bridge
- Test Point pins and LED indicators for most on-board power supplies
- User selectable XMC VPWR (+5 or +12) with current limiting
- Requires host-supplied +3.3V, +5V, +12V, and -12V
- Universal PCI signaling
- LM75 thermal sensor

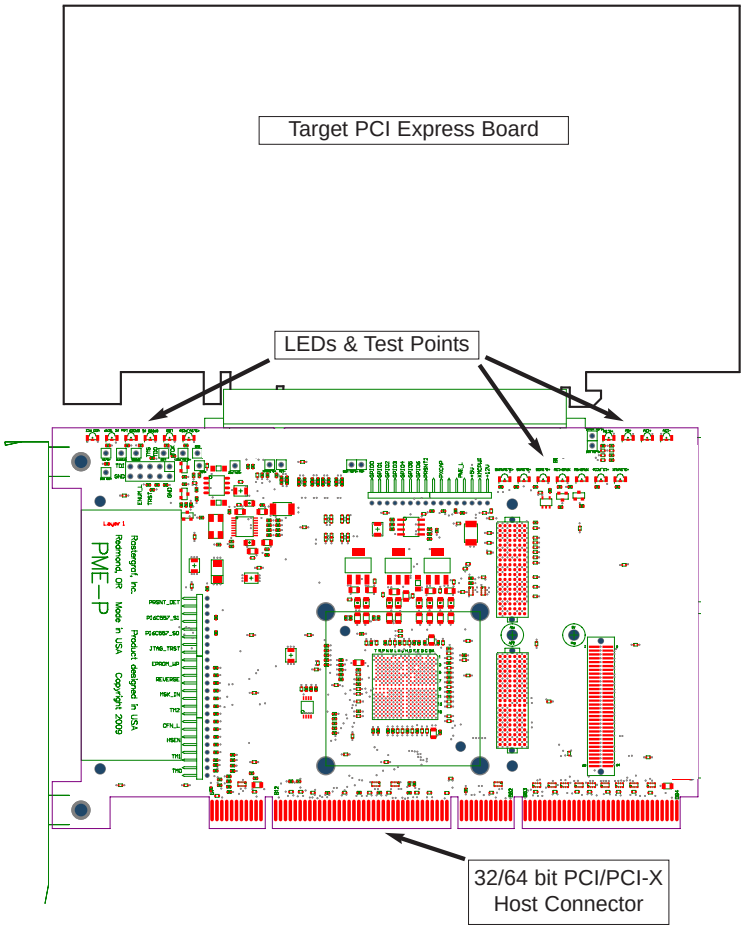
Figure 1-1 PMX-P Functional Outline



1.3 PME-P Feature Summary

- Short PCI board form factor
- 32/64-bit, 33/66/100/133 MHz PCI/PCI-X operation
- PCI 2.3 and PCI-X 1.0 compliant with Universal PCI signaling
- PCIe 1.1 specification compliant supports PCIe x1, x2, or x4
- Uses Pericom PI7C9X130 PCI Express to PCI/PCI-X Bridge
- PCIe socket accepts up to x16 (only up to x4 is actually connected)
- Test Point pins and LED indicators for most on-board power supplies
- Requires host-supplied +3.3V, +5V, +12V, and -12V
- PCIe hot-swap is not supported
- LM75 thermal sensor

Figure 1-2 PME-P Functional Outline



1.4 Additional References

You can find Rastergraf documentation and other technical literature on the Rastergraf web page (http://www.rastergraf.com).

The ***PCI Local Bus 2.3 Specification*** and the ***PCI-X1.0 Specification*** are maintained by the **PCI Special Interest Group** (PCISIG)

Web Page: http://www.pcisig.com/home

Some specifications are available from Rastergraf's technical library:

Web Page: http://www.rastergraf.com/Library/standards_library.htm

VITA Documentation Store:
Order any official VITA standard

https://www.vita.com/online-store.html

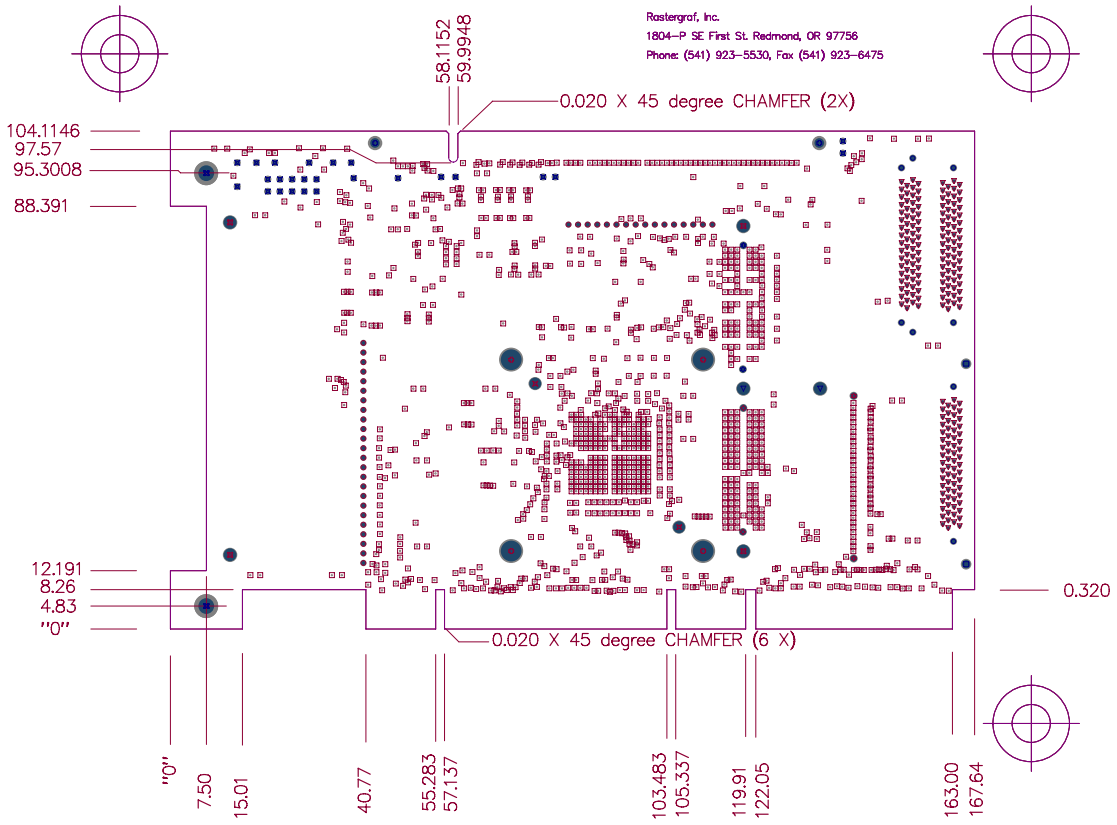
1156.2-1996:
IEEE Standard for Environmental Specifications for Computer Systems 1996 (includes IEEE 1101)

1156.2-1996 IEEE Standard for Environmental Specifications for Computer Systems

1386-2001 and 1386.1-2001:
IEEE Standard for a Common Mezzanine Card Family: CMC and IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards

1386-2001 & 1386.1 Standard for a Common Mezzanine Card Family

Chapter 2
Specifications



2.1 Specifications Common to the PMX-P and PME-P

Form Factor:	Short PCI, standard height: 167.7 mm x 104.1 mm.
PCI Interface:	Bridged connection uses PI7C9X130 PCI/PCI-X to PCIe (x1, x2, x4). PCI is 32/64 bit, 33/66 MHz. PCI-X is 32/64 bit, 33/66/100/133 MHz. Full PCI and PCI-X functionality was verified on a Supermicro C2SBX motherboard.
Indicators:	Green LEDs for 3.3VAUX, +12V_PCIe, 3.3V_PCIe, +12V, -12V, 5V, 3.3V, 1.8V_VAUXS, 1.8V_VDS, 1.8V_VAS, VIO PCI, LOO, XMC VPWR = +12V. Amber LED for GPIO3 high, XMC VPWR = 5V. Red for Hi Temp, GPIO3 Low
Test Points:	3.3VAUX, +12V_PCIe, 3.3V_PCIe, +12V, -12V, 5V, 3.3V, 1.8V_VAUXS, 1.8V_VDS, 1.8V_VAS, VIO PCI, LOO, XMC VPWR, Hi Temp, GPIO3, GND
Printed Circuit Board:	8 layer stackup: Signal, Ground, Signal, 3.3V, VDDC (PI7C9X130 Core), Signal, Ground, Signal PCI/PCI-X trace lengths (connector to PI7C9X130) by necessity exceed standard trace length specifications because the pinout for the PI7C9X130 is backwards from that which would yield the optimum trace layout. There is no other chip that would work better. Each PCIe CLK, R, and T nets pair is matched to +/- .125 mm. PCIe net pairs don't have to be matched pair to pair Signal traces are impedance controlled, verified with SPECCTRA advanced noise rules and simulated with less than 25 mV trace to trace, parallel or layer to layer.
Standards Compatibility:	PCI Revision 2.2 and PCI-X Revision 1.0.
PCI Bus Loading:	One PCI 2.2 compatible load
Power Requirements:	See Sections 2.2 and 2.3. Note that the PCI Host MUST supply 3.3V. Board PRSNT1/2 pins advertise as requiring up to 25W
Weight	0.26 kg (0.56 lb)
Environmental	Operating temperature: 0 to 70°C Storage: -40 to +85°C Humidity: 5 to 95% non-condensing

2.2 Specifications Unique to the PMX-P

Target Interface

One VITA 42.0 compliant XMC module.

The PMX-P uses the Samtec ASP-103612-04, which is the Low Insertion Force, lead-free (preinstalled) solder balls version (see Samtec Listing. It is designed to mate with the ASP-103614-04. See Section 4.3 for more information.

Due to features of the Samtec connector, there is a limit of approximately 75 – 100 insertion/removal cycles.

PCIe Access

Uses XMC Pn5. Follows VITA 42.3 Specification for PCI Express on XMC. Supports a single x1, x2, or x4 PCIe Gen1 connection. See Section 3.2 for more information.

I/O Access

XMC Front Panel and/or PMX-P breakout connectors which support PMC Pn4 to 68-pin VHDCI and XMC Pn6 to dual 68-pin VHDCI connectors:

The Pn4 breakout follows VITA 46.9 ***P64s*** pinout but the I/O connector is a 68-pin VHDCI. Signals are routed as 32 matched length pairs. The set of 32 pairs match length to within +/- .125 mm. Also see Section 3.1.

The Pn6 breakout follows VITA 46.9 ***x8+12d38s*** pinout but the I/O connector is ***two*** 68-pin VHDCIs. Signals are routed as 39 matched length pairs. The set of 39 pairs match length to within +/- .125 mm. Also see Section 3.3.

Standards Compatibility:

VITA 42.0 (XMC), **VITA 42.3** (PCIe on XMC), and parts of **VITA 46.9** (I/O), **PCIe Specification 1.1** for PCIe signal rules and connections.

Power Requirements:

Board: +/-12V @ 20 mA each (est)
5V @ 20 mA (est)
3.3V @0 .4A. (est)

Additional power will be consumed by the XMC module. The current/pin rating for the XMC is 1A. The XMC has 14 power pins: If VPWR = +12, you have a theoretical power of 133W! The practical power limit for an XMC is actually in the range of 15W to 20W. The PMX-P does not have current limiting on the +/-12V and 3.3V pins but this is subject to change in a later revision. However, XMC VPWR is current limited by a Polyswitch resettable fuse:

for VPWR = +5V, fuse is 2.6A Hold, 5A Trip, 5s trip time
+12V, fuse is 1.25A Hold, 2.5A Trip, .4s trip time

2.3 Specifications Unique to the PME-P

Target Interface	One PCIe Specification 1.1 (Gen 1) compliant PCIe module.
PCIe Access	Uses top mounted socket (see Figure 1-2) without card latch. Accepts x1 to x16 PCIe card, but bridge only goes up to x4. Supports a single x1, x2, or x4 PCIe Gen1 connection. See Section 3.4 for more information.
I/O Access	I/O area of PCIe target board. Note that in some cases, it may be necessary to remove the PCIe sheet metal panel in order to get things to fit.
Standards Compatibility:	PCIe Specification 1.1
Power Requirements:	Board: +/-12V @ 20 mA each 5V @ 20 mA 3.3V @0 .4A. Additional power is consumed by the PCIe module (+/-12V and 3.3V. Presently, no current limiting is enforced but this is subject to change in a later revision.

Chapter 3
Connector Pinouts

3.1 PMX-P Pn4 I/O Connector (PMX-P/P46)

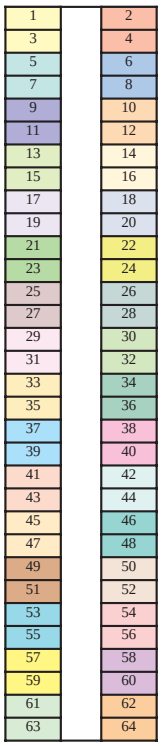
The PMC Pn4 Breakout Connector pinout is derived from the VITA 46.9 P64s pinout. Since the V46 connector is not appropriate for this product, the 64 pins are mapped as 32 differential pairs wired to a Honda HDRA-EC68LFDT-S-SL+ VHDCI (.8MM) connector.

The pair grouping on PMC Pn4 connector are adjacent pins on the same side of the connector (1,3; 2,4). The pairs are length matched both by pair and over the signal set at 28.425 mm +/- .125 mm (via to via).

Connections are routed as 100 ohm differential pairs.
If used as single-ended, one line in each pair MUST be grounded.

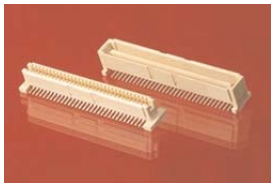
When used as differential pairs, 100 Ohm round cable (discrete twisted pair cable) MUST BE USED. Ribbon (IDC) cable CANNOT be used because routing limitations prevented matching circuit pairs with ribbon cable pairs.

PMC Pn4



PMC Pn4	VHDCI-68
	1, 35 GND
1, 3	2, 3
2, 4	36, 37
5, 7	4, 5
6, 8	38, 39
9, 11	6, 7
10, 12	40, 41
13, 15	8, 9
14, 16	42, 43
17, 19	10, 11
18, 20	44, 45
21, 23	12, 13
22, 24	46, 47
25, 27	14, 15
26, 28	48, 49
29, 31	16, 17
30, 32	50, 51
33, 35	18, 19
34, 36	52, 53
37, 39	20, 21
38, 40	54, 55
41, 43	22, 23
42, 44	56, 57
45, 47	24, 25
46, 48	58, 59
49, 51	26, 27
50, 52	60, 61
53, 55	28, 29
54, 56	62, 63
57, 59	30, 31
58, 60	64, 65
61, 63	32, 33
62, 64	66, 67
	34, 68 GND

VHDCI 68



Molex PMC Connectors

Honda HDRA-EC68LFDT VHCDCI Connector

3.2 PMX-P Pn5 Target (VITA 42.3/PCIe) Connector

Position	A	B	C	D	E	F
1	PCIe PERp0	PCIe PERn0	3.3V	PCIe PERp1	PCIe PERn1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PCIe PERp2	PCIe PERn2	3.3V	PCIe PERp3	PCIe PERn3	VPWR
4	GND	GND	TCK	GND	GND	(MRSTO#)
5	n/c	n/c	3.3V	n/c	n/c	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	n/c	n/c	3.3V	n/c	n/c	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	RFU	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PCIe PETp0	PCIe PETn0	(MBIST#)	PCIe PETp1	PCIe PETn1	VPWR
12	GND	GND	GA1	GND	GND	MPRES#
13	PCIe PETp2	PCIe PETn2	3.3Vaux	PCIe PETp3	PCIe PETn3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	n/c	n/c	RFU	n/c	n/c	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	n/c	n/c	RFU	n/c	n/c	RFU
18	GND	GND	RFU	GND	GND	RFU
19	REFCLK+	REFCLK-	RFU	(WAKE#)	(ROOT0#)	RFU

Notes: The table above follows PCIe Electromechanical Specification (PCIeES) naming conventions. Note that for some reason VITA 42.3 Section 4.2.3 swaps the R and T part of the data pair naming relative to the definition provided in PCIeES (1.1) Section 5.1:

"By default, PETpx and PETnx pins (the Transmitter differential pair of the connector) shall be connected to the PCI Express Transmitter differential pair on the system board, and to the PCI Express Receiver differential pair on the add-in card."

n/c = not connected., RFU = Reserved for Future Use
VPWR can be connected to +5 or +12. See Section 4.5 for more information about power
GA0, GA1, GA2, MPRES#, and MVMRO not used. Pulled up to 3.3V thru 5.1K
MRSTI# connected to PCI/PCI-X RESET#.
MRSTO#, MBIST#, WAKE#, and ROOT0# not connected
MSDA connected to PCI/PCI-X SDA, MSCL connected to PCI/PCI-X SCL
JTAG signals connected to PCI/PCI-X signals. JTAG I/O looped thru XMC board
3.3Vaux connected to PCI/PCI-X 3.3Vaux.

3.3 PMX-P Pn6 I/O Connector (PMX-P/P46)

The XMC Pn6 Breakout Connector pinout is is derived from the VITA 46.9 X8+12d38s pinout. Since the V46 connector is not appropriate, the 78 signal pins are mapped as 39 differential pairs wired to a Honda HDRA-E68W1LFDT1EC-SL+ VHDCI (.8MM) dual connector.

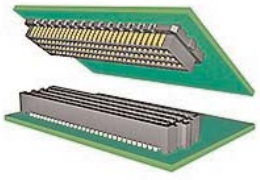
The pairs are length matched both by pair and over the signal set at 146.025 mm +/- .125 mm (via to via).

Connections are routed as 100 ohm differential pairs. If used as single-ended, one line in each pair MUST be grounded.

When used as differential pairs, 100 Ohm round cable (discrete twisted pair cable) MUST BE USED. Ribbon (IDC) cable CANNOT be used because routing limitations prevented matching circuit pairs with ribbon cable pairs.

XMC Pn6

A1	B1	C1	D1	E1	F1
A2	B2	C2	D2	E2	F2
A3	B3	C3	D3	E3	F3
A4	B4	C4	D4	E4	F4
A5	B5	C5	D5	E5	F5
A6	B6	C6	D6	E6	F6
A7	B7	C7	D7	E7	F7
A8	B8	C8	D8	E8	F8
A9	B9	C9	D9	E9	F9
A10	B10	C10	D10	E10	F10
A11	B11	C11	D11	E11	F11
A12	B12	C12	D12	E12	F12
A13	B13	C13	D13	E13	F13
A14	B14	C14	D14	E14	F14
A15	B15	C15	D15	E15	F15
A16	B16	C16	D16	E16	F16
A17	B17	C17	D17	E17	F17
A18	B18	C18	D18	E18	F18
A19	B19	C19	D19	E19	F19

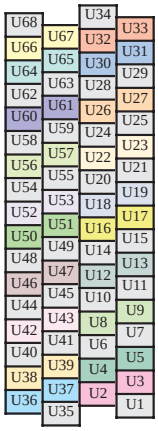


Samtec XMC Connectors

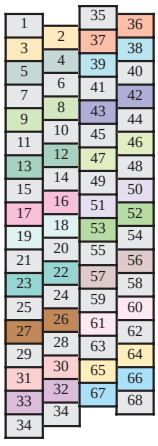
XMC Pn6	Upper VHDCI-68
A2, B2, D2, E2 - GND	U68, U34 - GND
A1, B1	U67, U66
D1, E1	U33, U32
A3, B3	U65, U64
D3, E3	U31, U30
A4, B4, D4, E4 - GND	U63, U62, U29, U28 - GND
A5, B5	U61, U60
D5, E5	U27, U26
A6, B6, D6, E6 - GND	U59, U58, U25, U24 - GND
A7, B7	U57, U56
D7, E7	U23, U22
A8, B8, D8, E8 - GND	U55, U54, U21, U20 - GND
A9, B9	U53, U52
D9, E9	U19, U18
A11, B11	U51, U50
D11, E11	U17, U16
A10, B10, D10, E10, A12, B12, D12, E12 - GND	U49, U48, U15, U14 - GND
A13, B13	U47, U46
D13, E13	U13, U12
A14, B14, D14, E14 - GND	U45, U44, U11, U10 - GND
A15, B15	U43, U42
D15, E15	U9, U8
A16, B16, D16, E16 - GND	U41, U40, U7, U6 - GND
A17, B17	U39, U38
D17, E17	U5, U4
A19, B19	U37, U36
D19, E19	U3, U2
A18, B18, D18, E18 - GND	U35, U1 - GND

XMC Pn6	Lower VHDCI-68
	1, 35 - GND
C1, F1	2, 3
n/c	36, 37
C2, C3	4, 5
F2, F3	38, 39
	6, 7, 40, 41 - GND
C4, C5	8, 9
F4, F5	42, 43
	10, 11, 44, 45 - GND
C6, C7	12, 13
F6, F7	46, 47
	14, 15, 48, 49 - GND
C8, C9	16, 17
F8, F9	50, 51
C10, C11	18, 19
F10, F11	52, 53
	20, 21, 54, 55 - GND
C12, C13	22, 23
F12, F13	56, 57
	24, 25, 58, 59 - GND
C14, C15	26, 27
F14, F15	60. 61
	28, 29, 62, 63 - GND
C16, C17	30, 31
F16, F17	64, 65
C18, C19	32, 33
F18, F19	66. 67
	34, 68 - GND

Upper VHDCI-68



Lower VHDCI-68



Honda HDRA-E68W1LFDT VHDCI Connector

3.4 PME-P PCI Express Target Connector

Pin	Signal Name		Signal Name	Pin
B1	PRSNT1#		+12V	A1
B2	+12V		+12V	A2
B3	+12V		+12V	A3
B4	GND		GND	A4
B5	SMCLK		TCK	A5
B6	SMDAT		TDI	A6
B7	GND		TDO	A7
B8	3.3V		TMS	A8
B9	TRST#		3.3V	A9
B10	3.3Vaux		3.3V	A10
B11	WAKE#		PERST#	A11
KEY				
B12	RESV		GND	A12
B13	GND		REFCLK+	A13
B14	PETp0		REFCLK-	A14
B15	PETn0		GND	A15
B16	GND		PERp0	A16
B17	PRSNT2#		PERn0	A17
B18	GND		GND	A18
End of x1 Connector				
B19	PETp1		RESV	A19
B20	PETn1		GND	A20
B21	GND		PERp1	A21
B22	GND		PERn1	A22
B23	PETp2		GND	A23
B24	PETn2		GND	A24
B25	GND		PERp2	A25
B26	GND		PERn2	A26
B27	PETp3		GND	A27
B28	PETn3		GND	A28
B29	GND		PERp3	A29
B30	RESV		PERn3	A30
B31	PRSNT2#		GND	A31
B32	GND		RESV	A32
End of x4 Connector				

3.4 PME-P PCI Express Target Connector (continued)

Pin	Signal Name	Signal Name	Pin
B33	n/c	RESV	A33
B34	n/c	GND	A34
B35	GND	n/c	A35
B36	GND	n/c	A36
B37	n/c	GND	A37
B38	n/c	GND	A38
B39	GND	n/c	A39
B40	GND	n/c	A40
B41	n/c	GND	A41
B42	n/c	GND	A42
B43	GND	n/c	A43
B44	GND	n/c	A44
B45	n/c	GND	A45
B46	n/c	GND	A46
B47	GND	n/c	A47
B48	PRSNT2#	n/c	A48
B49	GND	GND	A49
End of x8 Connector			
B50	n/c	RESV	A50
B51	n/c	GND	A51
B52	GND	n/c	A52
B53	GND	n/c	A53
B54	n/c	GND	A54
B55	n/c	GND	A55
B56	GND	n/c	A56
B57	GND	n/c	A57
B58	n/c	GND	A58
B59	n/c	GND	A59
B60	GND	n/c	A60
B61	GND	n/c	A61
B62	n/c	GND	A62
B63	n/c	GND	A63

3.4 PME-P PCI Express Target Connector (continued)

Pin	Signal Name		Signal Name	Pin
B64	GND		n/c	A64
B65	GND		n/c	A65
B66	n/c		GND	A66
B67	n/c		GND	A67
B68	GND		n/c	A68
B69	GND		n/c	A69
B70	n/c		GND	A70
B71	n/c		GND	A71
B72	GND		n/c	A72
B73	GND		n/c	A73
B74	n/c		GND	A74
B75	n/c		GND	A75
B76	GND		n/c	A76
B77	GND		n/c	A77
B78	n/c		GND	A78
B79	n/c		GND	A79
B80	GND		n/c	A80
B81	PRSNT2#		n/c	A81
B82	RESV		GND	A82
End of x16 Connector				

Notes: The table above follows PCIe Electromechanical Specification 1.1.

n/c = not connected., RESV = Reserved for Future Use
+3.3 and +12 are current limited on Rev 1 (not Rev 0). See Section 4.5 for more information about power
PERST# connected to PCI/PCI-X RESET#.
WAKE# connected to a pullup to 3.3Vaux.
3.3Vaux connected to PCI/PCI-X 3.3Vaux.
Hot Swap function not supported
SMDAT connected to PCI/PCI-X SDA, SMCLK connected to PCI/PCI-X SCL
JTAG signals connected to PCI/PCI-X signals. JTAG I/O looped thru PCIe board

3.5 PMX-P and PME-P PCI/PCI-X Host Connector

3.5.1 PCI/PCI-X Bus 32-Bit Connector

Pin	Signal Name		Signal Name	Pin
B1	-12V		TRST	A1
B2	TCK		+12V	A2
B3	GND		TMS	A3
B4	TDO		TDI	A4
B5	5V		5V	A5
B6	5V		INTA#	A6
B7	INTB#		INTC#	A7
B8	INTD#		5V	A8
B9	PRSNT1#		RESV	A9
B10	RESV		VIO	A10
B11	PRSNT2#		RESV	A11
B12	KEY			A12
B13				A13
B14	RESV		3.3Vaux	A14
B15	GND		PCIRST#	A15
B16	PCICLK		VIO	A16
B17	GND		GNT#	A17
B18	REQ#		GND	A18
B19	VIO		PMEL	A19
B20	AD[31]		AD[30]	A20
B21	AD[29]		3.3V	A21
B22	GND		AD[28]	A22
B23	AD[27]		AD[26]	A23
B24	AD[25]		GND	A24
B25	3.3V		AD[24]	A25
B26	CBE[3]#		IDSEL	A26
B27	AD[23]		3.3V	A27
B28	GND		AD[22]	A28
B29	AD[21]		AD[20]	A29
B30	AD[19]		GND	A30
B31	3.3V		AD[18]	A31
B32	AD[17]		AD[16]	A32

3.5.1 PCI/PCI-X Bus 32-Bit Connector (continued)

Pin	Signal Name		Signal Name	Pin
B33	CBE[2]#		3.3V	A33
B34	GND		FRAME#	A34
B35	IRDY#		GND	A35
B36	3.3V		TRDY#	A36
B37	DEVSEL#		GND	A37
B38	PCIXCAP		STOP#	A38
B39	LOCK#		3.3V	A39
B40	PERR#		SMCLK	A40
B41	3.3V		SMDAT	A41
B42	SERR#		GND	A42
B43	3.3V		PAR	A43
B44	CBE[1]#		AD[15]	A44
B45	AD[14]		3.3V	A45
B46	GND		AD[13]	A46
B47	AD[12]		AD[11]	A47
B48	AD[10]		GND	A48
B49	M66EN		AD[09]	A49
B50	KEY			A50
B51				A51
B52	AD[08]		CBE[0]#	A52
B53	AD[07]		3.3V	A53
B54	3.3V		AD[06]	A54
B55	AD[05]		AD[04]	A55
B56	AD[03]		GND	A56
B57	GND		AD[02]	A57
B58	AD[01]		AD[00]	A58
B59	VIO		VIO	A59
B60	ACK64#		REQ64#	A60
B61	5V		5V	A61
B62	5V		5V	A62
	KEY			

3.5.2 PCI/PCI-X Bus 64-Bit Connector Extension

Pin	Signal Name	Signal Name	Pin
B63	RESV	GND	A63
B64	GND	CBE[7]#	A64
B65	CBE[6]#	CBE[5]#	A65
B66	CBE[4]#	VIO	A66
B67	GND	PAR64	A67
B68	AD[63]	AD[62]	A68
B69	AD[61]	GND	A69
B70	VIO	AD[60]	A70
B71	AD[59]	AD[58]	A71
B72	AD[57]	GND	A72
B73	GND	AD[56]	A73
B74	AD[55]	AD[54]	A74
B75	AD[53]	VIO	A75
B76	GND	AD[52]	A76
B77	AD[51]	AD[50]	A77
B78	AD[49]	GND	A78
B79	VIO	AD[48]	A79
B80	AD[47]	AD[46]	A80
B81	AD[45]	GND	A81
B82	GND	AD[44]	A82
B83	AD[43]	AD[42]	A83
B84	AD[41]	VIO	A84
B85	GND	AD[40]	A85
B86	AD[39]	AD[38]	A86
B87	AD[37]	GND	A87
B88	VIO	AD[36]	A88
B89	AD[35]	AD[34]	A89
B90	AD[33]	GND	A90
B91	GND	AD[32]	A91
B92	RESV	RESV	A92
B93	RESV	GND	A93
B94	GND	RESV	A94

Chapter 4
Installing Your PMX-P or PME-P Board

4.1 Introduction

Using the PMX-P or PME-P involves resolving some system integration issues. The PMX-P is a carrier for an XMC card and the PME-P is an adapter for a PCIe card. In either case, of course, you have to know what you are doing and how you plan to use the board. The PMX-P allows you to install the XMC card and actually close up the system box. The PME-P is like an extender card, and in most cases there is no way to close up the box. To see the difference, please see Figures 1-1 and 1-2.

Please note that it is beyond the scope of this manual to deal with the selection and use of actual XMC or PCIe cards, solving their I/O problems, or software. We can only advise on the connection between them and the CPU host.

4.2 Comments Concerning XMC boards

XMC board specifications are bit of a mess. VITA 42.0 defines the XMC card form factor, differential pair locations on the connector, and some common signals. However, 42.0 doesn't require a particular use of the differential pairs. Several "dot", or subspecifications, do that, and even then things are not nailed down very well.

VITA 42.3 is used for implementing PCI Express (Gen1) on the XMC card. It envisions the possibilities of a single x1 to x16 link, or even two x1 to x8 links. This makes it IMPERATIVE that you know what your XMC board is designed to do BEFORE you plug it into the PMX-P.

The PMX-P is designed for use with XMC boards that have a single x1 to x4 PCIe port located on Pn5. It will work with an x8, but only x4 wide link will be active.

The second XMC connector, in location Pn6, is used only for I/O. It should not cause any harm to plug an x16 XMC board which would use lines on Pn6) into the PMX-P, but you still will have only an x4 PCIe connection. Please contact Rastergraf support if you have questions.

WARNING:

The PMX-P does NOT support Rapid I/O XMC boards. Damage to the PMX-P and/or a Rapid I/O (or other non-PCIe XMC) will likely result if you try to use such a board with the PMX-P.

There are other potential problems with the XMC:

a) The XMC uses a BGA-based 7x19 connector from Samtec. At the time of writing, this connector system has not been documented to be viable for more about 75 – 100 insertion/removal cycles. This is because of stress failures in the BGA solder joints. All of the mechanical stress of the connector system goes through the BGA solder joints and they are not strong enough to withstand many cycles. Please contact Rastergraf if you have questions or concerns about this.

b) The VITA 42.0 XMC master specification defines 14 power pins. The power/pin is rated at 1A. Given the various supply voltages, you could theoretically draw in excess of 130W. There is nothing in the VITA 42.0 specification that controls power consumption. Note that the practical limit of the XMC card with 10 mm spacing is around 15W to 20W. Please exercise caution. See Section 2.2 for more information.

4.3 Comments Concerning PCIe boards

PCIe cards are pretty straightforward. There is only one connector definition and it covers board implementations from x1 to x16 data links. It allows some optional features such as Hot Swap and JTAG.

PME-P will accept a board with anything from x1 to x16 PCIe. However, the intrinsic capability of the PI7C9X130 bridge is limited to a maximum of x4, so anything beyond that is ignored. Also, you can use either PCIe Gen1 (2.5Mb/s links) or Gen2 (5 Mb/s links). But the bridge is Gen1, so the data links will operate at 2.5Mbs. At the time of this writing, no standalone Gen2 PCI/PCIe bridge is commercially available.

It is unlikely that you will run into trouble trying to use any sort of PCIe card EXCEPT high-power graphics boards. The PME-P advertises to the PCI/PCI-X host on the PCI PRSNT1# and PRSNT2# pins that it is a 25 watt board, which means the host should supply that much. However, it is not clear than most systems actually limit power to the slots. ***Therefore, please exercise caution and don't try to run a board that needs more than 25 watts***.

4.4 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

> **Caution**
>
> Be careful not to remove the board from its antistatic bag or container until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

4.5 Changing Jumpers

In the following subsections, please refer ***Figure 4-1*** for jumper locations.

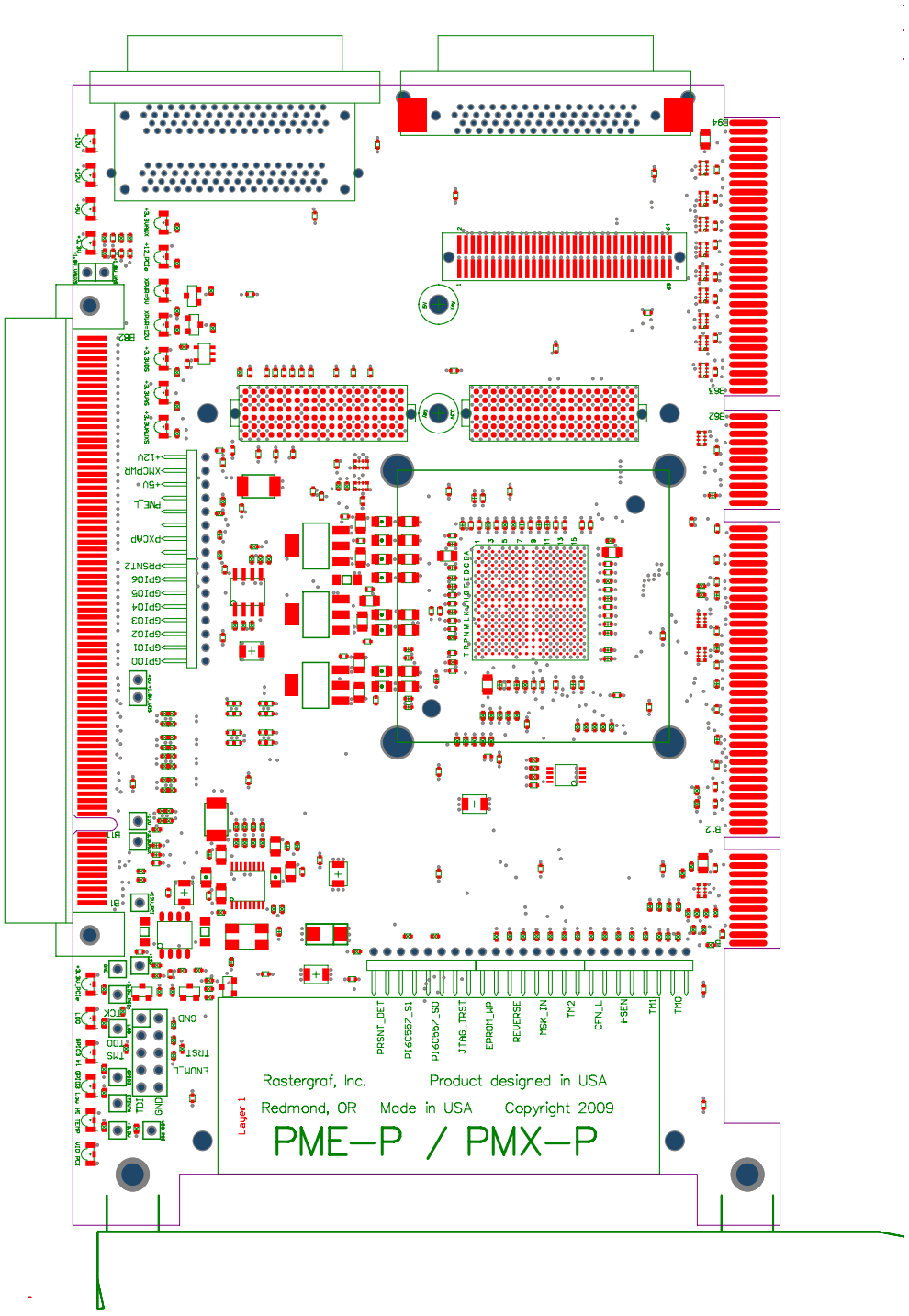
4.5.1 VPWR Select

The XMC specification provides for the eight VPWR pins on Pn5 to be set to +5V or +12V. **This means that you need to be VERY SURE of what your target XMC board expects on VPWR.** To be on the safe side, the PMX-P is shipped with NO JUMPER INSTALLED. Thus, there is 0 volts on the pins. **Rastergraf cannot be responsible for damage caused to your board if you select the wrong voltage. If you have any questions about what to do, please contact Rastergraf for assistance.**

4.5.2 EEPROM Write Enable

The PMX-P has an EEPROM that can be loaded with a variety of start-up parameters as well as manufacturing-related information. However, due to problems with Pericom's EEPROM program it is best not to use it. A jumper must be installed to allow the EEPROM to be reprogrammed.

Figure 4-1 Jumper Locations



Chapter 5
Troubleshooting

Introduction

This chapter contains information which should assist you in tracking down installation and functional problems with your board.

5.1 General procedures

5.2 Dealing with the PCI bus

5.3 Maintenance, Warranty, and Service

5.1 General Procedures

The PM Series boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. If the problem can not be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical PM Series will draw a total of less than 1 Amp at +5 and +3.3 Volts.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 5 Amps must be drawn from the +5 Volt supply before the +12 volt supplies will give the proper readings.

5.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the PM Series, it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf's software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

While x86 systems generally follow the standards required to meet PC compatibility and mask these details, PowerPC systems do not. Among PowerPC vendors, there are no standards which ensure interoperability among CPU boards, even when they use the same CPU and PCI bridge.

Therefore, if you plan to use an PM Series board in a PowerPC based system, it is vital to ensure that Rastergraf can vouch for the board's operation before you order the board. Otherwise, you may go crazy trying to figure out why it doesn't work. Please contact us at support@rastergraf.com or (541) 923-5530 if you have problems.

5.3 Maintenance, Warranty, and Service

Maintenance

The PM Series requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the board and other boards in the system, forced crossflow ventilation is required. If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

Warranty

The PM Series boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf's obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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