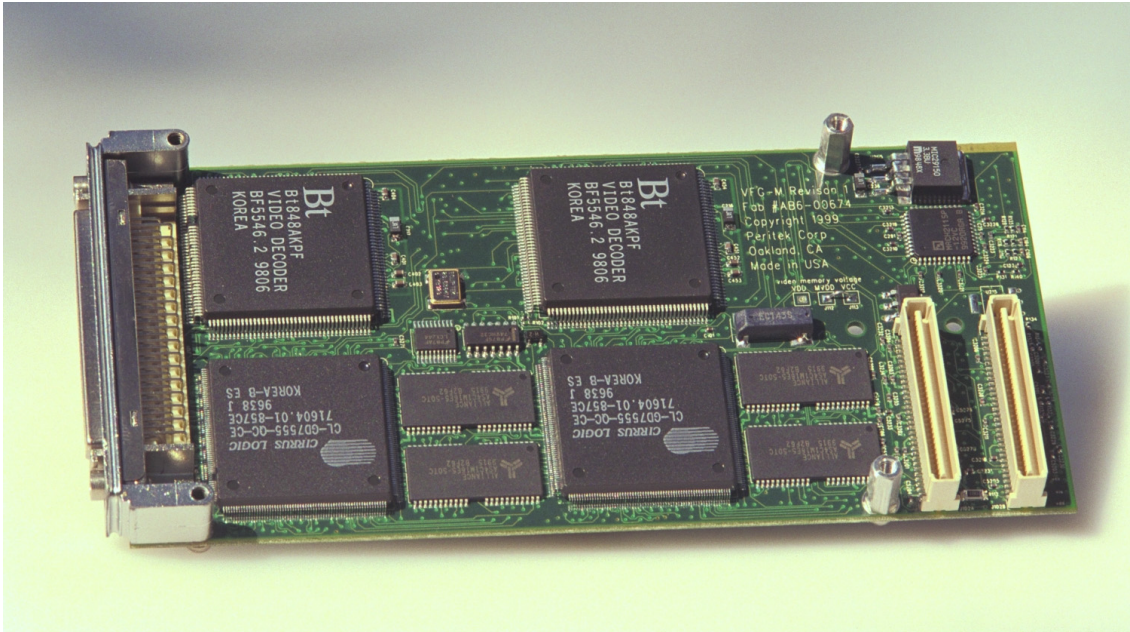# *Rastergraf*

# VFG-M
## Dual High Resolution Graphics Controllers with Dual Video Digitizers and Two-Port USB Controller



## Features

- Two independent 64-bit graphics accelerators
- 4 MB display memory per channel
- Supports displays up to 1280 x 1024 at 8, 16, or 24 bits/pixel
- Two independent NTSC/PAL video digitizers drive PCI bus and Cirrus Zoom Video Ports
- VGA and FCode BIOS
- Two channel USB 1.1 hub controller

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*Rastergraf - graphics boards for VME and PMC*

# The VFG-M

The Rastegraf **VFG-M** is a single PMC video input and graphics display controller for VMEbus and CompactPCI computers.

The VFG-M has a two channel *OPTi 82C861 FireLink* USB controller, two *Conexant Bt848A Media Decoders*, and two *Cirrus Logic CL-GD7555 Matterhorn* XVGA/SVGA compatible 64-bit graphics accelerators. The USB, Bt848As, and CL-GD7555s are isolated from the host PMC bus by a *Texas Instruments PCI2031* PCI-PCI bridge.

### XVGA Graphics

The CL-GD7555 XVGA Graphics Accelerator includes 64-bit BitBLT engine and and can yield performance in excess of 30M Winmarks.

One CL-GD7555 (Channel A) can function as the system VGA controller with on-board BIOS PROM. Otherwise, Channel B is identical and independent

The CL-GD7555 supports 8, 15, 16, and 24-bit true color modes and mapped RGB and YUV color formats. It includes a color-keyed overlay feature and a graphics cursor with a 64 x 64 x 2 bit map. DDC (display data channel) lines enable the computer to control the monitor.

Programmable timing registers control the video timing, supporting analog (RGBHV) output formats up to 1280 x 1024 x 24 bpp. Note: composite sync is not supported.

### Video Input

The **Bt848A** is a single-chip solution for analog signal capture on the PCI bus. An input multiplexer enables the BT848A to accept data from one of four inputs.

Each Bt848A is directly connected to a corresponding CL-GD7555's Zoom Video port, which allows video data to be overlaid into the display window. The Bt848A RISC-based DMA engine takes advantage of the PCI-based system's high bandwidth to transfer video data to other PCI devices.
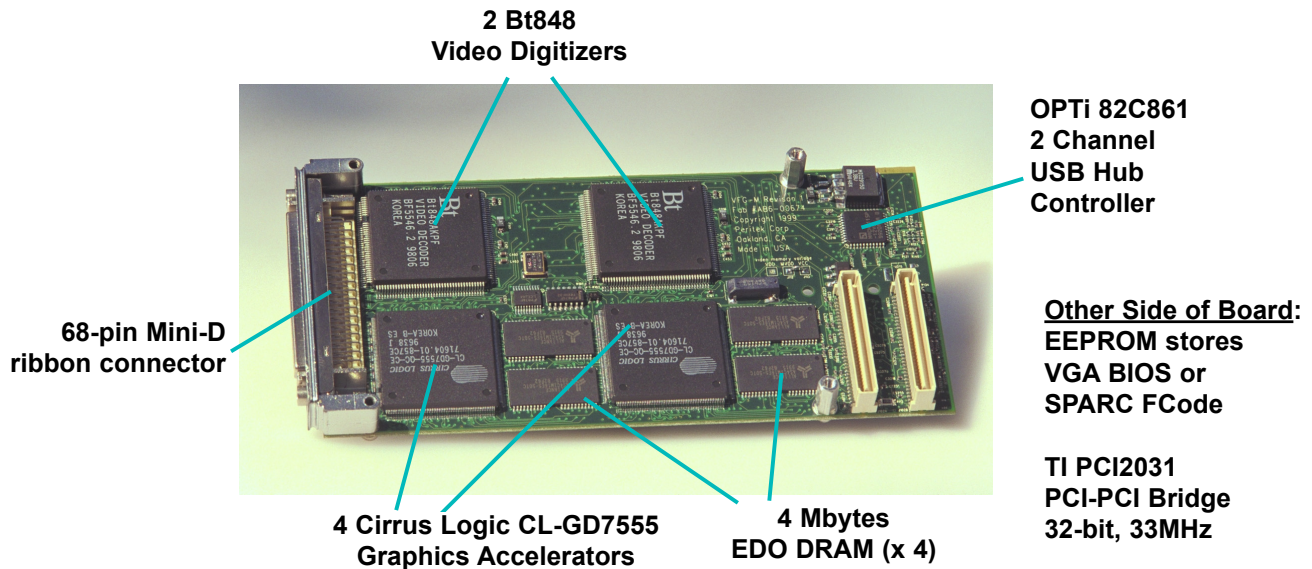
### USB

The VFG-M has a two channel USB hub controller for use with a number of devices, including mouse, trackball, keyboard, scanner, and video.

### I/O Connections

VFG-M I/O is available at the front panel 68-pin high density connector. A breakout cable splits the functions into two standard VGA connectors for graphics (RGBHV and DDC), two USB connectors, and two 15-pin VGA-style connectors for video input.

### PMC Form Factor

The PCI Mezzanine Card (PMC) implementation provides a modular graphics solution for VMEbus and other platforms that support the PMC specification.



**2 Bt848 Video Digitizers**

**OPTi 82C861 2 Channel USB Hub Controller**

**68-pin Mini-D ribbon connector**

**Other Side of Board:**
**EEPROM stores VGA BIOS or SPARC FCode**

**TI PCI2031 PCI-PCI Bridge 32-bit, 33MHz**

**4 Cirrus Logic CL-GD7555 Graphics Accelerators**

**4 Mbytes EDO DRAM (x 4)**

# VFG-M Features

- Two independent 64-bit graphics controllers
- Each display programmable for 8, 16, or 24 bits/pixel
- Each controller supported with 4 Mbytes EDO DRAM
- Supports Analog RGB output up to 1280 x 1024
- Programmable video timing
- Gamma correction
- Hardware scroll, pan, and cursor

- VGA support on Channel A
- Serial EEPROM on Channel A
- Two independent 64-bit graphics controllers
- Dual channel USB hub controller
- 33 MHz, 32-bit PCI interface

# VFG-M Technical Overview

The VFG-M features **Two** independent 50 MHz Cirrus Logic CL-GD7555s, which each include a 64-bit BitBLT engine, 64-bit memory interface, and 64-bit data paths, BitBLT setup register double buffering with autostart, transparent BitBLT (source color key), memory-mapped I/O, and programmable video timing. Multiple apertures in the 7555 enable interleaved graphics and video data blocks. VGA Compatibility is included. The maximum supported frequencies are 135 MHz for the pixel clock and 100 MHz for the memory clock.

The 4 MB DRAM display memory is 64-bits/word, byte addressable, no-wait state and gives three pages of 1280 x 1024 using 8-bit pixels, 1.5 pages using 16-bit pixels, or one page using packed 24 bpp mode.

A 64 KB EEPROM on Channel A is normally loaded with VGA BIOS or SPARC Fcode. A 2Kb Serial EEPROM (controlled by PCI2031 PIO bits) stores PCI2031 power-up, and Rastergraf and customer codes.

Display Output Features include an integral color lookup table (RAMDAC) with a 24-bit true-color palette and 8-bit DACs with support for gamma/color adjustment in High and True-Color modes. Integrated color space converter for 4:2:2 YCrCb to RGB 8:8:8. Hardware destination color and chroma-key support (hardware occlusion). Video format support for 24 and 16-bpp RG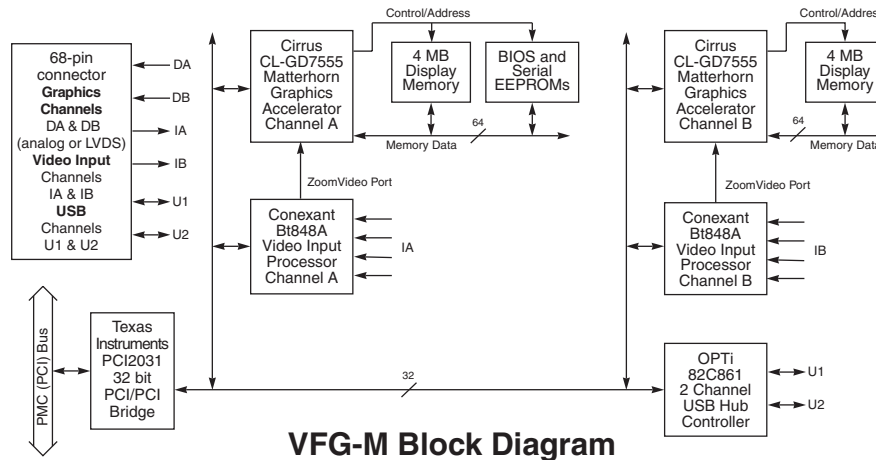B and 4:2:2 YCrCb. The RAMDAC has a 64 x 64 x 2 bitmap cursor. A color key can be used to switch the CLUT from passing the RGB components straight through to sampling the pixel to the color map, thus providing a mapped overlay value. Scroll on single line (smooth scroll) and pan anywhere on 8 pixel boundaries are supported.

The 7555 supports analog displays on 5 Wire (RGBHV) output up to 1280 x 1024 x 24 bpp. Composite sync on green is not available. Digital output is not currently supported.

A **2 Port USB1.1 Hub Controller** enabls the VFG-M to support a variety of peripherals. It uses a bus-mastering OPTi FireLink 82C861 USB hub controller. Output is differential data/clock and switched 5V.

VFG-M devices are accessed by PMC/PCI bus through a 33 MHz TI PCI2031 Transparent **PCI-PCI Bridge** which supports extended burst cycles and automatic bus retry for high data transfer rates.

**Two Bt848A Video** provide digitized NTSC, PAL, and SECAM video up to 768x576 (full PAL) to companion 7555 via ZoomVideo Port. Can also supply video stream to any PCI devices using integral DMA bus-master controller. Performs complex clipping and scaling of video source, no-wait state PCI burst writes, and field/frame masking to throttle bandwidth to target. Multiple YCrCb and RGB formats.



**VFG-M Block Diagram**

# SDL Overview

The Standard Drawing Library, SDL, is a scaleable C graphics library designed for use with real-time and non-real-time operating systems. SDL is small, compact, ROMable, and offers device independent graphics functions for board level and embedded systems applications.

SDL is easy to use and provides a complete set of graphics primitives. These graphics primitives can be extended by adding utility functions for specialized graphics tasks.

SDL is written in ANSI C and is supplied in library format, which means that its target code size can be controlled by limiting the number of functions used in a given application. SDL has been designed to run on any CPU and operating system that uses linear addressing and that is supported by an ANSI C compiler and linker.

# SDL Feature Summary

- Written in ANSI C - full Featured and Easy to Use
- Scaleable, ROMable, and Minimal RAM usage
- Solid (thin and wide) and Dashed Lines and Rectangles
- Circles, Ellipses, and Arcs
- Filled Circles, Chords, Sectors, and Polygons
- Solid and Pattern Fills

- Pixel Processing
- Proportional and Fixed Width Fonts
- Clipping Rectangle and Logical Origin
- Screen to Screen and Host to Screen Image Copy
- Mouse and Keyboard Support
- Video Capture Extensions

# VFG-M Product Specifications

| | |
|---|---|
| **Graphics Controllers** | Four Cirrus Logic CL-GD7555 Matterhorn |
| **Maximum Dot Clock** | 135 MHz |
| **Horizontal Scan Rates** | 31.5 to 115 KHz |
| **Display Resolution** | 1280 x 1024 (max.) |
| **Display Colors** | 16.7 Million @ 24-bpp, 256 @ 8-bpp |
| **Memory Configuration** | |
|    Display memory | 4MB EDO DRAM |
|    Serial EEPROM | 2KB |
| **Analog Monitor Support** | Multi-frequency (VGA type) monitors |
| **Flatpanel Support** | Analog with VGA compatible interface |
| **Video Input Controllers** | Two Conexant Bt848 |
| **Two Port USB Hub Controller** | Bus-mastering OPTi FireLink 82C861 USB 1.1 hub controller. Output is differential data/clock and switched 5V |
| **PCI-PCI Bridge** | 33 MHz TI PCI2031 Transparent PCI-PCI Bridge. Supports extended burst cycles and automatic bus retry. |
| **PMC Bus Compatibility** | IEEE P1386.1 and PCI 2.1 compliant. Universal PCI Bus signaling (5V and 3.3V). 32-bit (J1 only). |
| **PMC (PCI) Interrupts and IDSELs** | 7555 (Ch A) INTA, IDSEL = PCIAD16<br>7555 (Ch B) INTB, IDSEL = PCIAD17<br>848 (Ch A) INTC, IDSEL = PCIAD18<br>848 (Ch B) INTD, IDSEL = PCIAD19<br>USB: INTA, IDSEL = PCIAD20 |
| **PCI Subsystem Vendor ID** | 0x10F0 |
| **PCI Subsystem Device ID** | 0xB600 (VFG-M Identifier) |
| **Front Panel Connections** | 68-pin 3M N10268-52E2VC Mini-D ribbon connector. |
| **Adapter cable** | |
|    Video Outputs | Two each Red, Green, Blue, and TTL level DDC, vertical, and horizontal sync on a VGA connector. |
|    Video Inputs | Each channel: one-of-four composite or one S-Video plus one-of-three composite inputs on a VGA connector. Use a VGA-to-5-BNC cable access individual video lines. |
|    USB I/O | Two standard USB Type A connectors. |
| **Multiple Display Support** | Multiple VFG-M boards may be added to a single system. |
| **Power-management capabilities** | Provides Suspend, Standby, and power down control of select unused 7555 functions. DDC-2B lines control the monitor. |
| **VFG-M Maintenance Features** | Red, Amber, and Green LEDs can be used for diagnostics by customer software.<br><br>The 7555 can report valid monitor connections. |
| **Software Support** | Windows NT/2K<br><br>Linux/XFree86 and Solaris SunX DDX<br><br>Standard Drawing Library (SDL) for Linux and VxWorks<br><br>Rastergraf provides both VGA BIOS and FCode firmware options for the VFG-M. |
| **Environment** | |
|    Operating temperature | 0°C to +60°C |
|    Storage temperature | -55°C to +85°C |
|    Humidity | 10% - 90% non-condensing |
| **Power Requirements** | +5V ±5%, 1.5 A typical |
| **Dimensions** | IEEE 1386 PMC, 149mm x 74mm |

# Display Resolutions

| Resolution | Vertical Scan Rate | | | |
|---|---|---|---|---|
| | Windows and RTOS | | Solaris | |
| | Format | Frequency | Index | Frequency |
| 640 x 480 | VGA | 60 Hz<br>75 Hz | 8<br>9 | 60 Hz<br>75 Hz |
| 800 x 600 | SVGA | 60 Hz<br>75 Hz | 6<br>7 | 60 Hz<br>75 Hz |
| 1024 x 768 | UVGA | 60 Hz<br>75 Hz | 0<br>1 | 60 Hz<br>75 Hz |
| 1152 x 864 | Sun | 60 Hz<br>75 Hz | 2 [default]<br>3 | 60 Hz<br>75 Hz |
| 1280 x 1024 | SXGA | 60 Hz | 4 | 60 Hz |

# Ordering Information

**VFG-M**

Two Cirrus Logic CL-GD7555 Graphics Accelerators, 4 MB EDO DRAM (x4), hardware pan, scroll, and zoom, 2-bit cursor and analog (RGBHV) output, two Conexant Bt848 video digitizers, and dual channel USB Hub controller. Includes VGA BIOS.

**VFG-M/F**

As above but with FCode BIOS.

**MVU-6/3**

68-pin MDSM to 2 x VGA display, 2 x VGA type connector for video input, and 2 x USB "Type A" breakout cable. Use separate VGA-to-5-BNC cables to access video in lines on the VGA connectors.

**Software:**

**DDX/SO/Rx.x**

DDX drivers for Solaris 2.6, 7 and 8.

**SDL/R3.6**

Standard Drawing Library (SDL): C-callable graphics library for use with VxWorks for PowerPC and Linux for x86.

**Note**: Version number may change as enhancements and improvements occur.

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